WHAT IS CLAIMED IS:

1. A circuit for testing a transceiver, comprising:

a test pattern generator configured to generate a test pattern;

a multiplexer having an input and an output, said input being capable of receiving said test pattern;

a demultiplexer coupled to said output of said multiplexer; and

a test result evaluation circuit configured to compare a signal from an output of said demultiplexer to said test pattern.

2. The circuit according to claim 1, wherein said test pattern generator is a linear feedback shift register.

3. The circuit according to claim 1, wherein said test pattern is a pseudo-random bit sequence.

4. The circuit according to claim 1, further comprising:

a clock/data recovery circuit coupled between said multiplexer and demultiplexer and configured to recover data from said output of said multiplexer and relay said recovered data to an input of said demultiplexer.

5. The circuit according to claim 2, wherein said test pattern has a corresponding signature.

6. The circuit according to claim 1, wherein said test result evaluation circuit further comprises:

a signature analyzer configured to analyze a corresponding signature of said signal;

a compare logic function coupled to said signature analyzer; and

a result recorder configured to record a result of said compare logic function.

7. The circuit according to claim 6, wherein said compare logic function comprises an AND circuit.

8. The circuit according to claim 6, wherein said signature analyzer further comprises:

a signature recorder controller configured to control when said signal is to be recorded;

a signature recorder configured to record said signal and generate said corresponding signature of said signal, said signature recorder being coupled to and controlled by said signature recorder controller; and

a signature comparator configured to compare said corresponding signature of said signal with a signature of said test pattern.

9. The circuit according to claim 8, wherein said signature recorder is a linear feedback shift register.

10. The circuit according to claim 6, wherein said result recorder is a flip-flop.

11. The circuit according to claim 1, wherein said circuit and said transceiver are integrated into an integrated circuit.

12. An improved circuit for testing a transceiver having a multiplexer and a demultiplexer, said improved circuit comprising:

a test pattern generator configured to generate a test pattern and coupled to an input of said multiplexer; and

a test result evaluation circuit configured to compare a signal from an output of said demultiplexer to said test pattern;

wherein an output of said multiplexer is coupled to an input of said demultiplexer.

13. The improved circuit according to claim 12, wherein said improved circuit is incorporated with said transceiver into an integrated circuit.

14. The improved circuit according to claim 11, wherein said test pattern generator is a linear feedback shift register.

15. The improved circuit according to claim 11, wherein said test result evaluation circuit further comprises:

a signature recorder controller configured to control recording of said signal;

a signature recorder configured to record said signal and generate a corresponding signature based on said signal, said signature recorder being coupled to and controlled by said signature recorder controller; and

a signature comparator configured to compare said corresponding signature with a signature of said test pattern.

16. The improved circuit according to claim 15, wherein said signature recorder is a linear feedback shift register.

17. A built-in self-testing circuit for testing an integrated circuit having a transceiver, comprising:

a test pattern generator configured to generate a test pattern;

a multiplexer having a plurality of inputs and an output, said test pattern generator being coupled to said plurality of inputs;

a demultiplexer having an input and a plurality of outputs, said input of said demultiplexer being coupled to said output of said multiplexer; and

a test result evaluation circuit configured to receive said plurality of outputs of said demultiplexer.

18. The circuit according to claim 17, wherein said test pattern generator is a linear feedback shift register having a parallel output.

19. The circuit according to claim 18, wherein said parallel output is coupled to said plurality of inputs of said multiplexer.

20. The circuit according to claim 17, wherein said test pattern is fed into each of said plurality of inputs of said multiplexer.